

Testing and Programming the Integrator/ Digitizer Card for the Beam Loss Monitoring System

Prakrit Shrestha
Supervisor: Craig Drennan

The College of Wooster
Wooster Ohio 44691

Fermi National Accelerator Laboratory
Batavia Illinois 60510

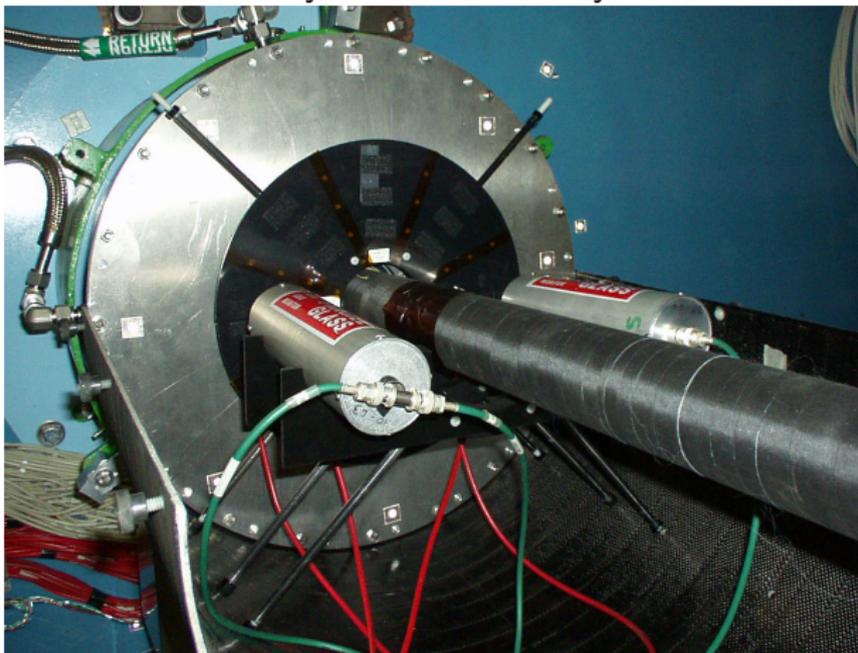
SIST Program

August 5, 2013

- 1 The Beam Loss Monitoring System
- 2 Integrator/ Digitizer Card
- 3 Programming the Board
- 4 Testing the Module
- 5 Conclusion and Future Work

Introduction

In a perfect system, installing a BLM system would be illogical and unnecessary, however since we do not possess such a machine, it is necessary to install this system.

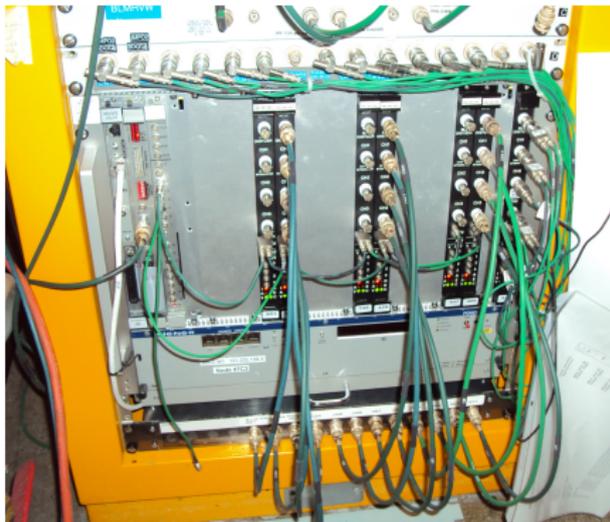


Ion Chamber



- Nickel Electrodes
- 110cm³ Argon gas
- Calibration: 70nC/Rad

VME crate



- Control Card
- Timing Card
- Abort Card
- High Voltage Card
- Digitizer Card

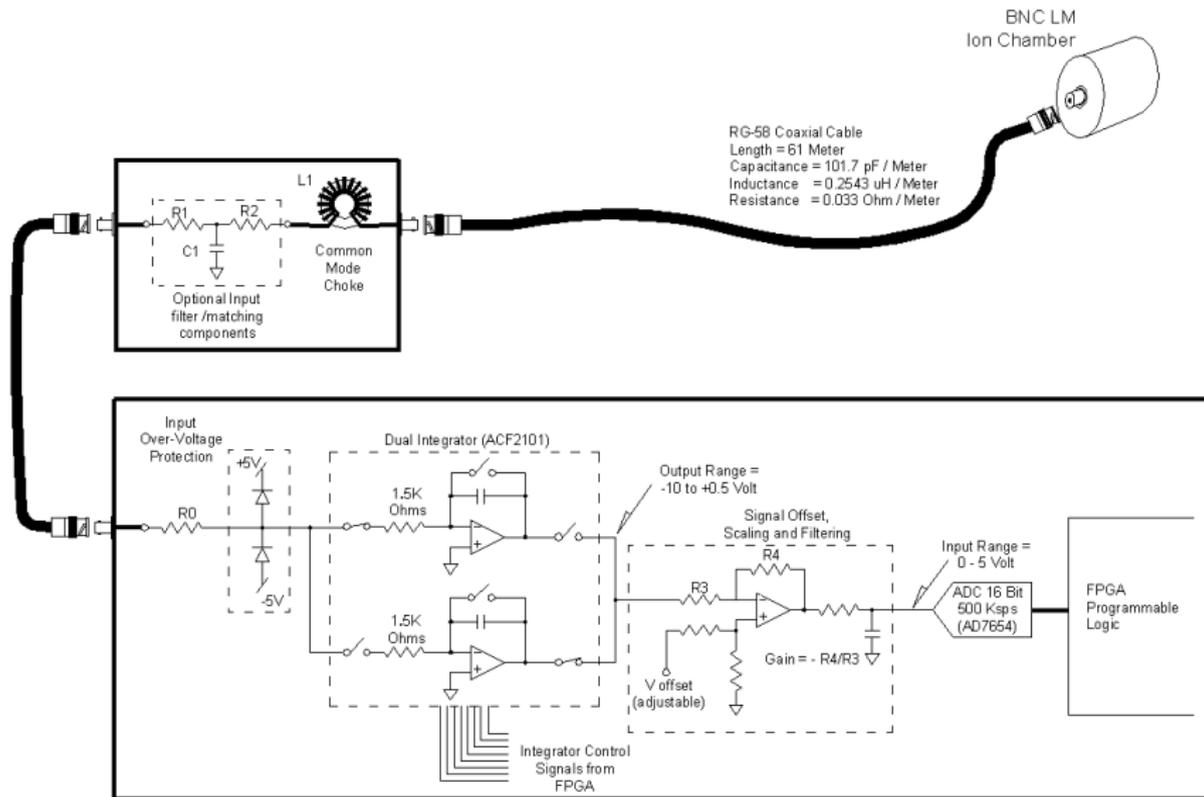
Outline

- 1 The Beam Loss Monitoring System
- 2 **Integrator/ Digitizer Card**
- 3 Programming the Board
- 4 Testing the Module
- 5 Conclusion and Future Work

4 Channel Integrator/ Digitizer



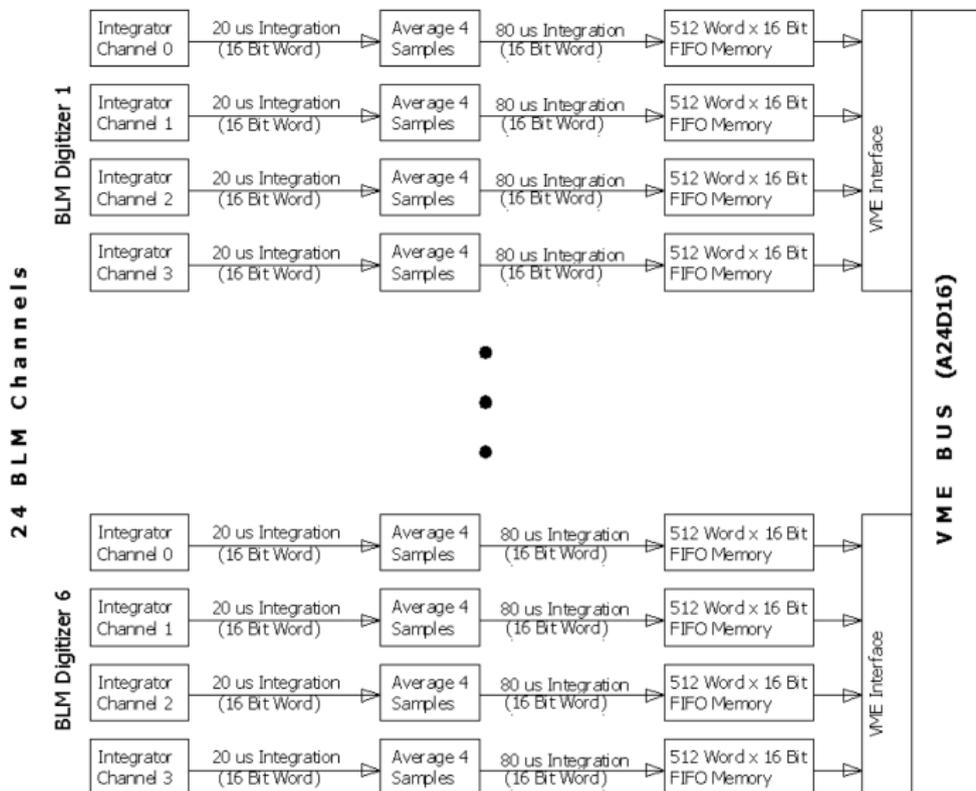
How does it work?



Components of the Module

- Dual Integrator, integration for 20 μ s,
- Analog to Digital Converter(ADC) produces a 16 bit word (1 bit \approx 15.26fC),
- Sum 4 sets of 20 μ s integration samples to get a 80 μ s sum,
- Divide the 80 μ s sums by 4 to get 16 bit word,
- Data Acquisition for 40 ms produces 500 samples/cycle,
- 500 samples written to FIFO,
- Samples transferred over the VME bus for analysis.

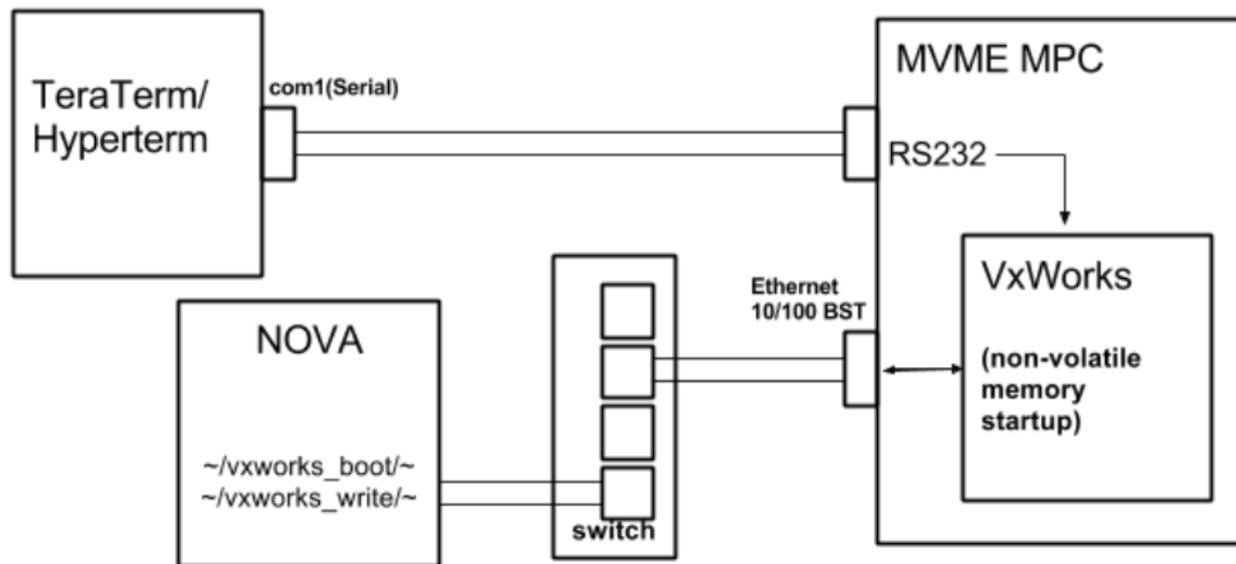
On Board Processing



Outline

- 1 The Beam Loss Monitoring System
- 2 Integrator/ Digitizer Card
- 3 Programming the Board**
- 4 Testing the Module
- 5 Conclusion and Future Work

Communication with the Board



FPGA (Field Programmable Gate Array)

Two FPGAs employed:

Upper/ INTEG

- manages sequencing and readout of integrator channels
- performs scaling and averaging of readings

Lower/ SUMS

- DAC analog outputs

FPGAs manufactured by Altera.

Code written and manufactured using Quartus (*.pof).

A *.bst file created using ATMEL programming system.

FPGA configured from the EEPROM device at each power up.

4 Channel Integrator/ Digitizer



Menu Mode

```
Tera Term - COM1 VT
File Edit Setup Control Window Help
# Enter 'menuvme' to open menu for testing UME!!
# Enter 'help' for help!!
#-----
Done executing startup script vxworks_boot/fe/blrfd3/startup
BLRFD3->menufpga
#-----
#
# 0. Exit
#
# 1. Read EEPROM and store data to file
#
# 2. Compare data file and EEPROM data
#
# 3. Config EEPROM from file
#
# 4. Read EEPROM, store data to file then verify
#-----
Enter choice (0-4): 1
Enter board index (0 for default): 0
Enter FPGA (1 for upper, 2 for lower): 1
Enter New File Name with extension: /remote/fpgaUp.bst
Board Index: 0
FPGA Type: INTEG
File Name:/remote/fpgaUp.bst
READ DCINTEG 0xfa000000
--> Write file /remote/fpgaUp.bst
24: 0xab --> Number of conguration bytes read: 200000
Enter choice (0 to exit, 5 to display menu):
```

Programming the FPGA

Command Line Mode

```
Tera Term - COM1 VT
File Edit Setup Control Window Help
# That's All Folks !!!
#-----
#      Enter 'menufpga' to open menu for programming FPGA!!
#      Enter 'cmd' to enter command line environment for programming FPGA!!
#      Enter 'menume' to open menu for testing UME!!
#      Enter 'help' for help!!
#-----
Done executing startup script vxworks_boot/fe/blrfd3/startup
BLRFD3->cmd
#-----
#                               SYNTAX FOR COMMANDS
# Config EEPROM from file::          wrt <iBoard> <type> <verify> <fname>
# Read EEPROM and store data to file::  prg <iBoard> <type> <fname>
# Compare data file and EEPROM data::  vfy <iBoard> <type> <fname>
# Read EEPROM, store data to file then verify:: prgofy <iBoard> <type> <fname>
#
# type= 1 (DCINTEG, upper fpga) or 2 (DCSUMS, lower fpga)
# fname = pointer to a filename string
# verify= 0 (load without a verify) or 1 (load then verify)
#
#      (*for detail information: enter command help*)
#-----
>wrt 0 1 1 upper130722.bst
Board Index: 0
FPGA Type: INTEG
Verify: YES
File Name: /remote/upper130722.bst

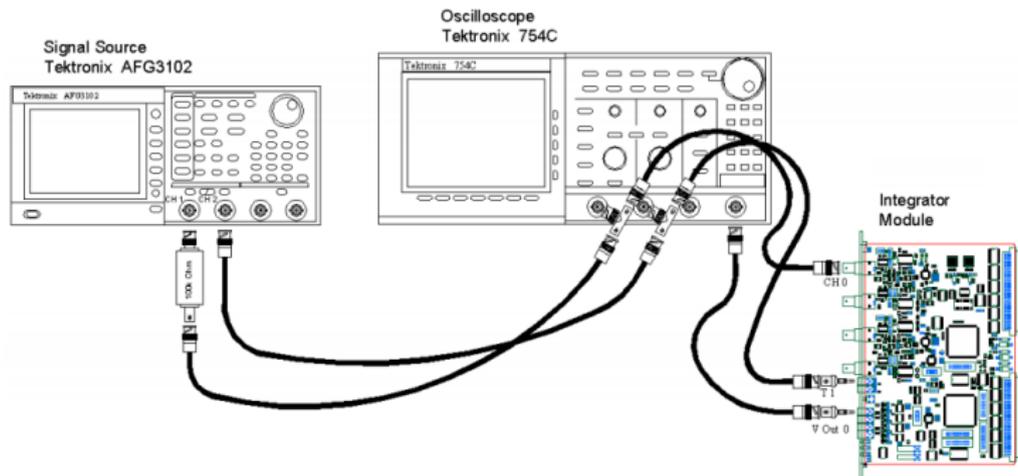
24: 0xab 11010101
BURN DCINTEG 0xfa000000
VERIFIED --> Number of conuguration bytes written: 78310
>exit
Have a nice day ! :)
value = 21 = 0x15
BLRFD3->
```

Outline

- 1 The Beam Loss Monitoring System
- 2 Integrator/ Digitizer Card
- 3 Programming the Board
- 4 **Testing the Module**
- 5 Conclusion and Future Work

Testing the Digitizer Card

Test with External Pulse



Test DAC (Digital to Analog Converter)

- Send analog signal from the Board
- Turn off all external input
DIP switch and Registers employed to work with code
- Write certain values to registers at certain address to send commands
example: write 0xff00 to register at address offset 0x01034 turns off FP input and turns on DAC input
- Data acquisition method is same
- Compare FIFO data to test DAC settings to evaluate Integrator and Digitizer

ROM Test

- Fixed values from ROM memory skips integration and digitization and stored to FIFO
- Data stored in FIFO is compared to expected data file computed from the known ROM values

Testing the Digitizer Card

Screenshot of Test

```
Tera Term - COM1 VT
File Edit Setup Control Window Help
Done executing startup script vxworks_boot/fe/blrfd3/startup
BLRFD3->menuvme

      === Setting up for Booster Operation ===

All integrations have been stopped.
All FIFOs have been cleared.

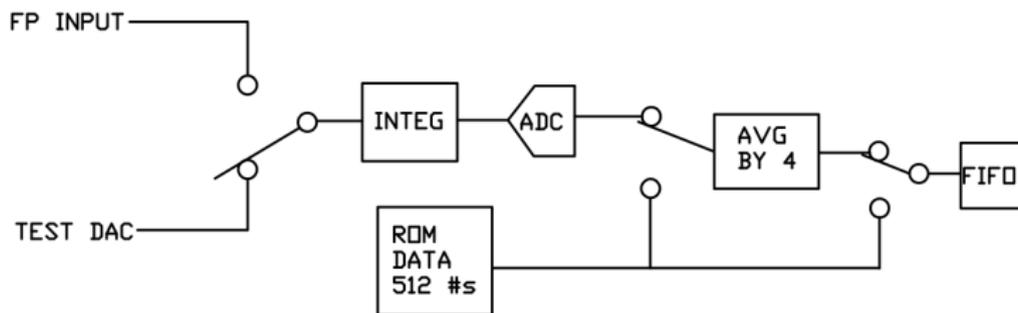
-----
##
## 0=Quit
## 1=Full ROM Test      2=Full test DAC
## 3=Set Test DAC      4=Run/Stop Integ
## 5=Read/Write FIFO   6=Expert Mode
##
-----
Input Choice: 6
6. Expert Mode
-----

      === Low Level Menu ===

##
## 0=Quit              1=Full ROM Test      2=Display Register Status
## 3=Set Test DAC     4=Run Integ          5=Stop Integ
## 6=Clear FIFOs      7=Test FIFO         8=Read/Write FIFO
## 9=Save Registers   10=Restore Registers 11=Read Register
## 12=Read & Modify Registers 13=Move Memory to Buffer 14=Move Buffer to Memory
## 15=Test Data from ROM
##
-----
Input Choice:
```

Testing the Digitizer Card

Schematic for Data Acquisition



Outline

- 1 The Beam Loss Monitoring System
- 2 Integrator/ Digitizer Card
- 3 Programming the Board
- 4 Testing the Module
- 5 Conclusion and Future Work

Conclusion and Future Work

- built user interface to program the FPGA
 - built routines to evaluate the veracity of the module
-
- build routines to test specific components of the board
 - multi-board FPGA programming
 - multi-board testing

Acknowledgements

- Craig C Drennan (Supervisor, Super Thanks)
- Elliott S McCrory
- Bradly T Verdant
- Dianne M Engram
- Linda M Diepholz
- Dr. Davenport
- ...entire SIST team

References

-  R. E. Shafer et al., *Comments on the Tevatron BLM System*, Fermilab BEAMS-DOC-790, July 2003.
-  R. E. Shafer et al., *A Tutorial on Beam Loss Monitoring*, in proceedings of Beam Instrumentation Workshop (NIW02), pp. 44-58, 6-9 May 2002, Upton, New York, USA.
-  A. Baumbaugh et al., *Beam Loss Monitor Upgrades at Fermi National Accelerator Laboratory*, August 2011.
-  C. Drennan, *Booster Beam Loss Monitor Data Acquisition and Presentation Specification*. Fermilab BEAM-DOCS-3723, December 2011.
-  J. Lackey, C. Drennan *Booster Wire Scanner Integrator*. Fermilab BEAMS-DOC-3723, October 2009.
-  C. Drennan, *Interfacing to the Booster BLM Upgrade Integrator/Digitizer VME Module*. Fermilab BEAM-DOCS-3780, February 2011.

Questions?